KAMAYA OHM

No.: RAAW–K–HTS–0001 /5
Date: 2025. 2. 14

Data sheet

Title: FIXED CHIP RESISTOR NETWORKS; RECTANGULAR TYPE & ANTI-SULFURATION

Style: RAAW06 2D, RAAW06 4D

RoHS COMPLIANCE ITEM
Halogen and Antimony Free

Note: ・Stock conditions
Temperature: +5°C ~ +35°C
Relative humidity: 25% ~ 75%
The period of guarantee: Within 2 year from shipment by the company.
Solderability shall be satisfied.
・Product specification contained in this data sheet are subject to change at any time without notice
・If you have any questions or a Purchasing Specification for any quality Agreement is necessary, please contact our sales staff.

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Drawing by: M. Shibuya

1. Scope

1.1 This data sheet covers the detail requirements for fixed chip resistor networks; rectangular type, style of RAAW06 2D, RAAW06 4D.

1.2 Applicable documents

JIS C 5201–1: 2011, JIS C 5201–9: 2006, JIS C 5201–9–1: 2006
IEC60115–1: 2008, IEC60115–9: 2004, IEC60115–9–1: 2004

2. Classification

Type designation shall be the following form.

(Example) 1.

RAAW	06	4	D	103	J	E	TH
1	2	3	4	5	6	7	8
	Style						

2.

RAAW	06	4	D	JP	E	TH
1	2	3	4	5	7	8
	Style					

1 Fixed chip resistor networks; rectangular type
2 Size
3 Number of elements
4 Circuits
} Style

5 Rated resistance

103	E24 Series, 3 digit, Ex. 103--> 10kΩ,
JP	Chip jumper

6 Tolerance on rated resistance

F	±1%
J	±5%

7 Terminal style

E	Convex Type	Flat Type Low profile (Face down)
G		Flat Type Low profile (Face up)

8 Packaging form

TH	Paper taping

3. Rating

The ratings shall be in accordance with Table–1.

3.1 Resistor

Table–1(1)

Style	Terminations style	Rated element dissipation (W)	Temperature coefficient of resistance (10^{-6} / °C)	Rated resistance range(Ω)	Preferred number series for resistors	Tolerance on rated resistance
RAAW06 2D	E, G	0.031	±200	100~100k	E24	F(±1%)
			±200	30~1M		J(±5%)
			±350	10~27		
RAAW06 4D	E, G		±200	100~100k	E24	F(±1%)
			±200	30~1M		J(±5%)
			±350	10~27		

Style	Limiting element voltage(V)	Insulation voltage(V)	Number of elements	Circuit networks	Category temperature range(°C)
RAAW06 2D	12.5	50	2	D (Independence type)	–55~+155
RAAW06 4D			4		

3.2 Chip Jumper

Table–1(2)

Style	Chip jumper symbol	Resistance value of chip jumper	Rated current of chip jumper(A)
RMC1/32	JP	50mΩmax.	1
RMC1/20			

3.3 Climatic category

55/155/56	Lower category temperature	–55 °C
	Upper category temperature	+155 °C
	Duration of the damp heat, steady state test	56days

3.4 Stability class

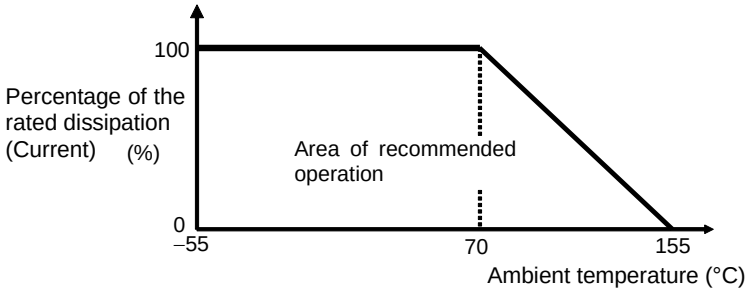
5%

Limits for change of resistance:

–for long–term tests	±(5%+0.1Ω)	Chip jumper: 50 mΩ max.
–for short–term tests	±(1%+0.05Ω)	Chip jumper: 50 mΩ max.

3.5 Derating

The derated values of dissipation (or current rating in case of chip jumper) at temperature in excess of 70 °C shall be as indicated by the following curve.



Figure–1Derating curve

3.6 Rated voltage

d. c. or a. c. r. m. s. voltage calculated from the square root of the product of the rated resistance and the rated dissipation.

$$E = \sqrt{P \cdot R}$$

E : Rated voltage (V)
P : Rated dissipation (W)
R : Rated resistance (Ω)

Limiting element voltage can only be applied to resistors when the resistance value is equal to or higher than the critical resistance value.

At high value of resistance, the rated voltage may not be applicable.

4. Packaging form

The standard packaging form shall be in accordance with Table–2.

Table–2

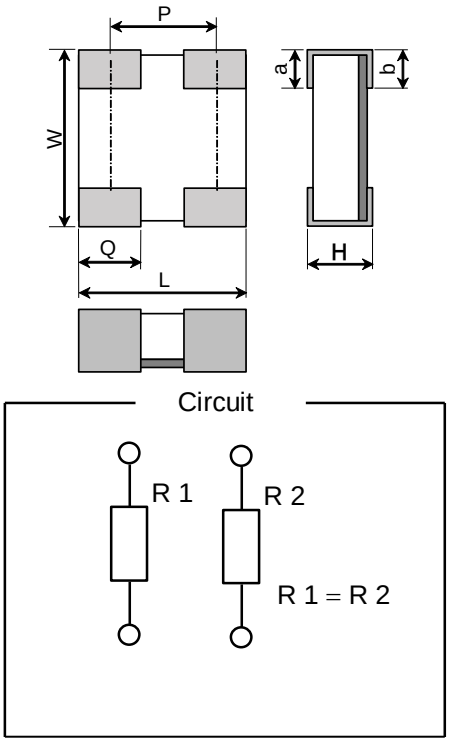
Symbol	Packaging form		Standard packaging quantity / units
TH	Paper taping	8mm width, 2mm pitches	10,000 pcs.

5. Dimensions

The resistor shall be of the design and physical dimensions in accordance with below.

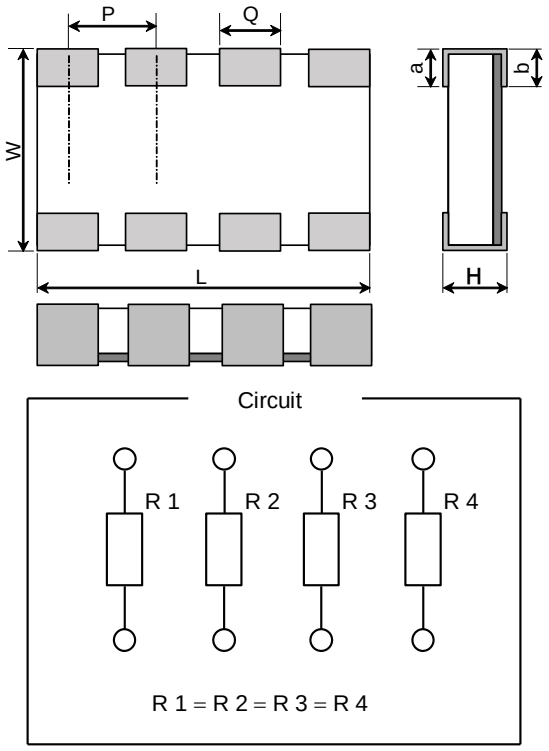
5.1 Terminations style:E.[Flat Type Low profile (Face down)]

5.1.1 RAAW06 2D



Figure–2

5.1.2 RAAW06 4D



Figure–3

Table–3 Unit: mm

Style	Terminations style	L	W	H	*Q	a	b	*P
RAAW06 2D	E	0.8±0.05	0.6±0.05	0.23±0.10	0.2±0.1	0.2±0.1	0.2±0.1	0.5
RAAW06 4D	E	1.4±0.05	0.6±0.05	0.23±0.10	0.2±0.1	0.2±0.1	0.2±0.1	0.4

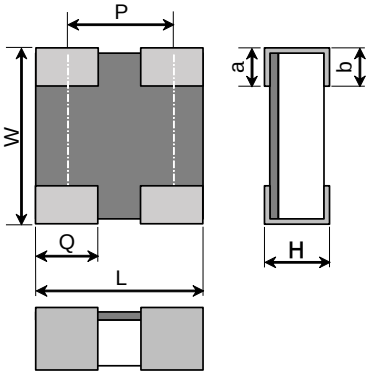
*Reference

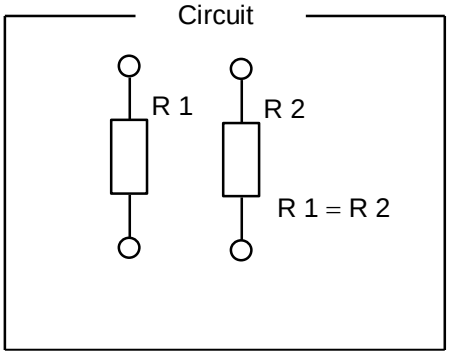
5.1.3 Net weight (Reference)

Style	Terminations style	Net weight(mg)
RAAW06 2D	E	0.38
RAAW06 4D	E	0.65

5.2 Terminations style:G.[Flat Type Low profile (Face up)]

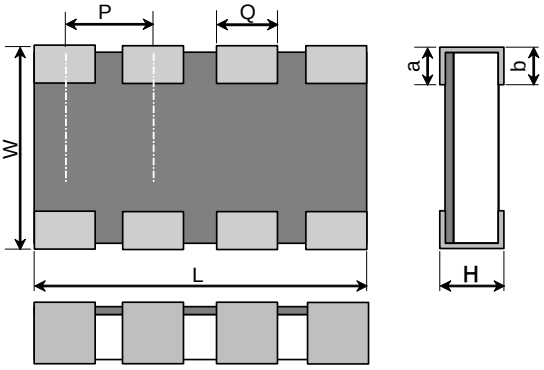
5.2.1 RAAW06 2D

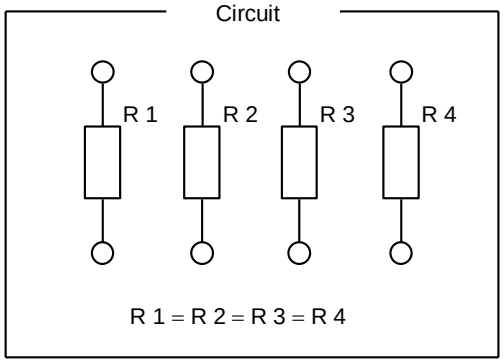




Figure–4

5.2.2 RAAW06 4D





Figure–5

Table–4 Unit: mm

Style	Terminations style	L	W	H	∗Q	a	b	∗P
RAAW06 2D	G	0.8±0.05	0.6±0.05	0.23±0.10	0.2±0.1	0.2±0.1	0.2±0.1	0.5
RAAW06 4D	G	1.4±0.05	0.6±0.05	0.23±0.10	0.2±0.1	0.2±0.1	0.2±0.1	0.4

∗Reference

5.2.3 Net weight (Reference)

Style	Terminations style	Net weight(mg)
RAAW06 2D	G	0.38
RAAW06 4D	G	0.65

6. Marking

The Rated resistance of RAAW06 2D, 4D should not be marked.

7. Performance

7.1 The standard condition for tests shall be in accordance with Sub–clause 4. 2, JIS C 5201–1: 2011.

7.2 The performance shall be satisfied in Table–5.

Table–5(1)

No.	Test items	Condition of test (JIS C 5201–1)	Performance requirements
1	Visual examination	Sub–clause 4. 4. 1 Checked by visual examination.	As in 4. 4. 1 The marking shall be legible, as checked by visual examination.
2	Dimension Resistance	Sub–clause 4. 4. 2 Sub–clause 4. 5	As specified in sub clause5 of this specification. As in 4. 5. 2 The resistance value shall correspond with the rated resistance taking into account the specified tolerance. Chip jumper: 50 mΩ max.
3	Voltage proof	Sub–clause 4. 7 Method: 4. 6. 1. 4 Test voltage: Alternating voltage with a peak value of 1.42 times the insulation voltage. Duration: 60 s ± 5 s Insulation resistance Test voltage: Insulation voltage Duration: 1 min.	No breakdown or flash over R ≥ 1 G Ω
4	Solderability	Sub–clause 4. 17 Without ageing Flux: The resistors shall be immersed in a non–activated soldering flux for 2s. Bath temperature: 235 °C ± 5 °C Immersion time: 2 s ± 0.5 s	As in 4. 17. 4. 5 The terminations shall be covered with a smooth and bright solder coating.
5	Mounting Overload (in the mounted state) Solvent resistance of the marking	Sub–clause 4. 31 Substrate material: Epoxide woven glass Sub–clause 4. 13 The applied voltage shall be 2.5 times the rated voltage or twice the limiting element voltage, whichever is the less severe. Duration: 2 s Visual examination Resistance Sub–clause 4. 30 Solvent: 2–propanol Solvent temperature: 23°C±5°C Method 1 Rubbing material: cotton wool Without recovery	 No visible damage Δ R ≤ ± (1%+0.05Ω) Chip jumper: 50 mΩ max. Legible marking

Table–5(2)

No	Test items	Condition of test (JIS C 5201 - 1)	Performance requirements
6	Mounting Bound strength of the end face plating Final measurements	Sub–clause 4. 31 Substrate material: Epoxide woven glass Sub–clause 4. 33 Bent value: 3 mm Resistance Sub–clause 4. 33. 6 Visual examination	 $\Delta R \leq \pm$ (1%+0.05Ω) Chip jumper: 50 mΩ max. No visible damage
7	Resistance to soldering heat Component solvent resistance	Sub–clause 4. 18 Solder temperature: 260°C±5°C Immersion time: 10s±0.5s Visual examination Resistance Sub–clause 4.29 Solvent: 2–propanol Solvent temperature: 23°C±5°C Method 2 Recovery: 48 h Visual examination Resistance	 As in 4. 18. 3. 4 No sign of damage such as cracks. $\Delta R \leq \pm$ (1%+0.05Ω) Chip jumper: 50 mΩ max. No visible damage $\Delta R \leq \pm$ (1%+0.05Ω) Chip jumper: 50 mΩ max.
8	Mounting Adhesion Rapid change temperature	Sub–clause 4. 31 Substrate material: Epoxide woven glass Sub–clause 4. 32 Force: 3 N Duration: 10s±1s Visual examination Sub–clause 4.19 Lower category temperature : –55 °C Upper category temperature : +155 °C Duration of exposure at each temperature: 30 min. Number of cycles: 5 cycles. Visual examination Resistance	 No visible damage No visible damage $\Delta R \leq \pm$(1%+0.05Ω) Chip jumper: 50 mΩ max.

Table–5(3)

No	Test items	Condition of test (JIS C 5201 - 1)	Performance requirements
9	Climatic sequence –Dry heat –Damp heat, cycle (12+12hour cycle) First cycle –Cold –Damp heat, cycle (12+12hourcycle) Remaining cycle –D.C. load	Sub–clause 4. 23 Sub–clause 4. 23. 2 Test temperature: +155 °C Duration: 16 h Sub–clause 4. 23. 3 Test method : 2 Test temperature: 55 °C [Severity(2)] Sub–clause 4. 23. 4 Test temperature–55 °C Duration: 2h Sub–clause 4. 23. 6 Test method: 2 Test temperature: 55 °C [Severity (2)] Number of cycles: 5 cycles Sub–clause 4. 23. 7 The applied voltage shall be the rated voltage or the limiting element voltage whichever is the smaller. Duration: 1 min. Visual examination Resistance	No visible damage $\Delta R \leq \pm$ (5%+0.1Ω) Chip jumper: 50 mΩ max.
10	Mounting Endurance at 70 °C	Sub–clause 4. 31 Substrate material: Epoxide woven glass Sub–clause 4. 25. 1 Ambient temperature: 70°C±2°C Duration: 1000 h The voltage shall be applied in cycles of 1. 5 h on and 0. 5 h off. The applied voltage shall be the rated voltage or the limiting element voltage whichever is the smaller. Examination at 48 h , 500 h and 1000 h: Visual examination Resistance	No visible damage $\Delta R \leq \pm$ (5%+0.1Ω) Chip jumper: 50 mΩ max.

Table–5(4)

No	Test items	Condition of test (JIS C 5201 - 1)	Performance requirements
11	Mounting Variation of resistance with temperature	Sub–clause 4. 31 Substrate material: Epoxide woven glass Sub–clause 4. 8 –55 °C / +20 °C +20 °C / +155°C	 As in Table–1
12	Mounting Damp heat, steady state	Sub–clause 4. 31 Substrate material: Epoxide woven glass Sub–clause 4. 24 Ambient temperature: 40°C±2°C Relative humidity : 93 $^{+2}_{-3}$ % a) 1st group: without voltage applied. b) 2nd group: The d. c. voltage shall be applied continuously. The voltage shall be accordance with Sub–clause 4. 24. 2 .1 b). without polarizing voltage [4. 24. 2. 1, c)] Visual examination Resistance	 No visible damage Legible marking $\Delta R \leq \pm (5\%+0.1\Omega)$ Chip jumper: 50 mΩ max.
13	Dimensions (detail) Mounting Endurance at upper category temperature	Sub–clause 4. 4. 3 Sub–clause 4. 31 Substrate material: Epoxide woven glass Sub–clause 4. 25. 3 Ambient temperature:155°C±2°C Duration: 1000 h Examination at 48 h, 500 h and 1000 h: Visual examination Resistance	As in Sub–clause 5 of this specification No visible damage $\Delta R \leq \pm (5\%+0.1\Omega)$ Chip jumper: 50 mΩ max.
14	Humid Sulfur vapor test (FOS)	ASTM B809 Reagent: Sulfur (Saturated vapor) Test temp.: 60°C Relative humidity: 95%RH Test period: 1000 h Resistance	 $\Delta R \leq \pm (1\%+0.05\Omega)$ Chip jumper: 50 mΩ max.

8. Taping

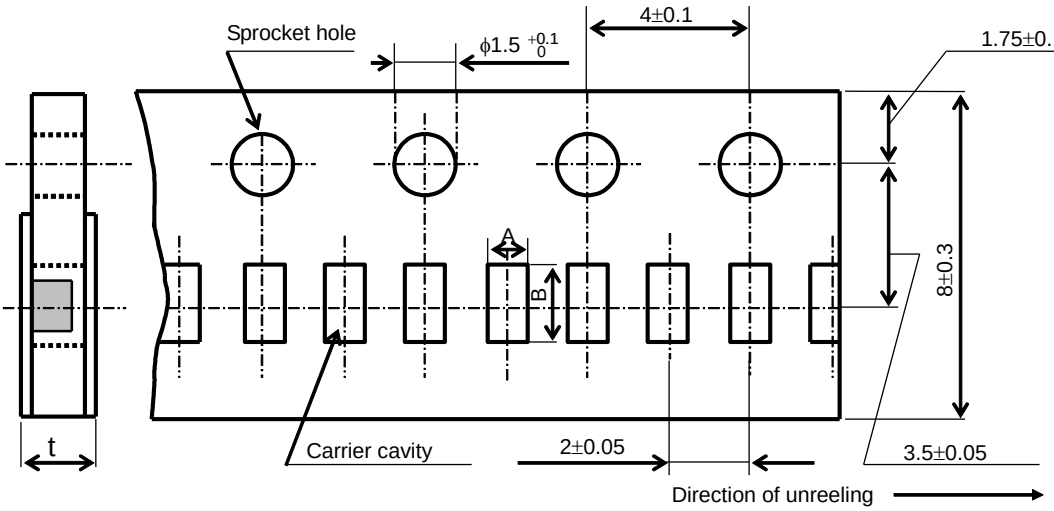
8.1 Applicable documents JIS C 0806–3: 2014, EIAJ ET–7200C: 2010

8.2 Taping dimensions

8.2.1 Paper taping (8mm width, 2mm pitches)

Taping dimensions shall be in accordance with Figure–6 and Table–6.

Unit: mm



Figure–6

Table–6 Unit: mm

Style	A	B	t
RAAW06 2D	0.7±0.1	0.9±0.1	0.6 max.
RAAW06 4D	0.7±0.1	1.5±0.1	

1). The cover tapes shall not cover the sprocket holes.

2). Tapes in adjacent layers shall not stick together in the packing.

3). Components shall not stick to the carrier tape or to the cover tape.

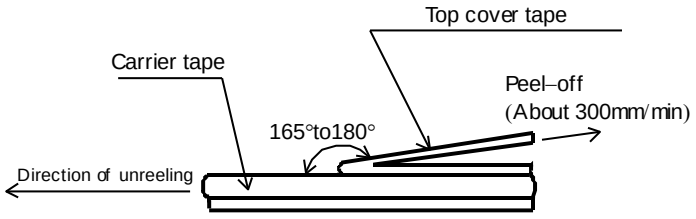
4). Pitch tolerance over any 10 pitches ±0.2mm.

5). The peel strength of the top cover tape shall be with in 0.1N to 0.5N on the test method as shown in the following Figure–7.

6). When the tape is bent with the minimum radius for 25 mm, the tape shall not be damaged and the components shall maintain their position and orientation in the tape.

7). In no case shall there be two or more consecutive components missing.
The maximum number of missing components shall be one or 0.1%, whichever is greater.

8). The resistors shall be faced to upward at the over coating side in the carrier cavity.

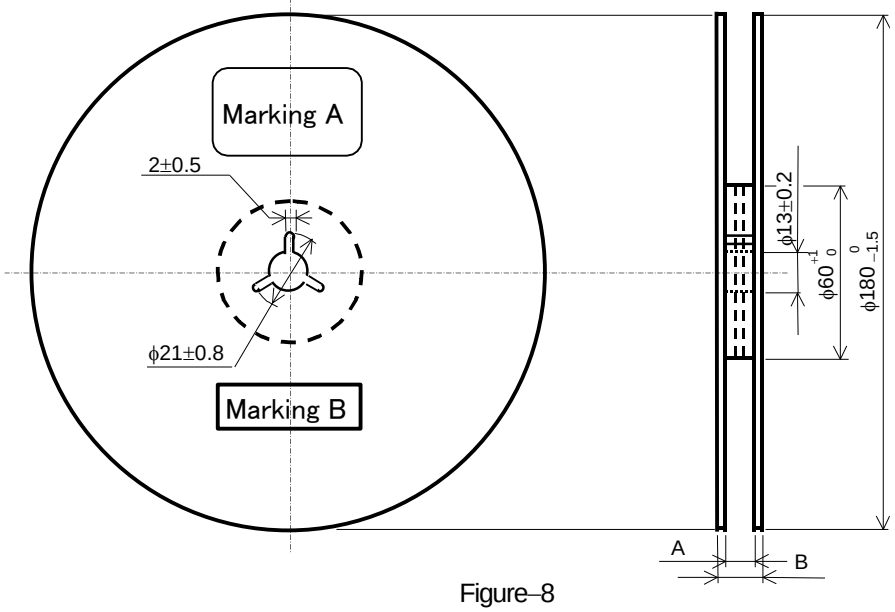


Figure–7

8.3 Reel dimension

Reel dimensions shall be in accordance with the following Figure−8 and Table−7.

Plastic reel (Based on EIAJ ET−7200C) Unit: mm



Figure−8

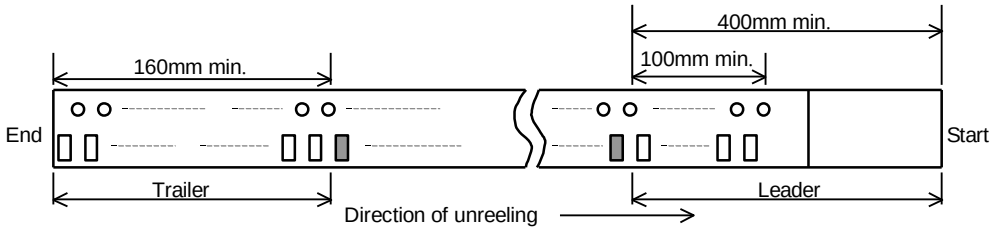
Table−7 Unit: mm

Style	A	B	Note
RAAW06	9 +1.0 0	11.4±1.0	Injection molding
		13±1.0	Vacuum forming

Note: Marking label shall be marked on a place of Marking A or two place of marking A and B.

8.4 Leader and trailer tape.

(Example)



Figure−9

9. Marking on package

The label of a minimum package shall be legibly marked with follows.

9.1 Marking A

(1) Classification (Style, Rated resistance, Tolerance on rated resistance, Terminal style, Packaging form)

(2) Quantity (3) Lot number (4) Manufacturer's name or trade mark (5) Others

9.2 Marking B (KAMAYA Control label)