KAMAYA OHM

No.:	RMAW–K–HTS-0001 /5
Date:	2023. 1. 17

Data sheet

Title: FIXED THICK FILM CHIP RESISTORS; RECTANGULAR TYPE & ANTI-SULFURATION

Style: RMAW06

RoHS COMPLIANCE ITEM
Halogen and Antimony Free

Note: ・Stock conditions
Temperature: +5°C ~ +35°C
Relative humidity: 25% ~ 75%
The period of guarantee: Within 2 year from shipment by the company.
Solderability shall be satisfied.

・Product specification contained in this data sheet are subject to change at any time without notice

・If you have any questions or a Purchasing Specification for any quality agreement is necessary, please contact our sales staff.

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1. Scope

1.1 This data sheet covers the detail requirements for fixed thick film chip resistors; rectangular type & anti-sulfuration, style of RMAW06.

1.2 Applicable documents

JIS C 5201−1: 2011, AEC-Q200 Rev.D

2. Classification

Type designation shall be the following form.

(Example) 1)

RMAW	06	K	123	J	PA
1	2	3	4	5	6
Style					

2)

RMAW	06	JP	PA
1	2	4	6
Style			

1 Fixed thick film chip resistors; rectangular type & anti-sulfuration

2 Rated dissipation and / or dimension

Style

3 Temperature coefficient of resistance

K	±100×10⁻⁶/ °C
−(Dash)	Standard

4 Rated resistance Example

123	E24 Series, 3 digit, Ex. 123--> 12kΩ,
1000	E96 Series, 4 digit, Ex. 1000-->100Ω 1022--> 10.2kΩ
JP	Jumper chip

5 Tolerance on rated resistance

D	±0.5%
F	±1%
J	±5%

6 Packaging form

B	Bulk (loose package)
PA	Press pocket taping

3. Rating

3.1 The ratings shall be in accordance with Table–1.

Table–1(1)

Style	Rated dissipation (W)	Temperature coefficient of resistance (10^{-6} / °C)		Rated resistance range (Ω)	Preferred number series for resistors	Tolerance on rated resistance
RMAW06	0.05	K	±100	51~1M	E24, 96	D(±0.5%), F(±1%)
		–(Dash) Standard	±200	1.02M~10M		F(±1%)
			±200	10~49.9		D(±0.5%), F(±1%)
			+600~–200	1~9.76		F(±1%)
		K	±100	51~1M	E24	J(±5%)
		–(Dash) Standard	±200	1.1M~10M		
			±200	10~47		
			+600~–200	1~9.1		

Style	Limiting element voltage (V)	Max. Overload voltage(V)	Category temperature range (°C)
RMAW06	25	50	–55~+155

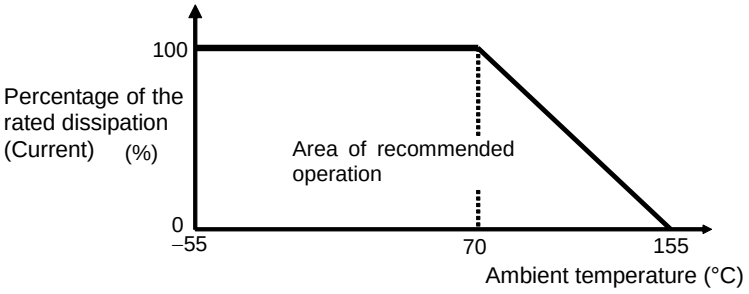
3.2 Chip Jumper

Table–1(2)

Style	Chip jumper symbol	Resistance value of chip jumper	Rated current of chip jumper (A)
RMAW06	JP	50mΩmax.	1

3.3 Derating

The derated values of dissipation (or current rating in case of chip jumper) at temperature in excess of 70 °C shall be as indicated by the following curve.



Figure–1 Derating curve

3.4 Rated voltage

d. c. or a. c. r. m. s. voltage calculated from the square root of the product of the rated resistance and the rated dissipation.

$$E = \sqrt{P \cdot R}$$

E : Rated voltage (V)
P : Rated dissipation (W)
R : Rated resistance (Ω)

Limiting element voltage can only be applied to resistors when the resistance value is equal to or higher than the critical resistance value.

At high value of resistance, the rated voltage may not be applicable.

4. Packaging form

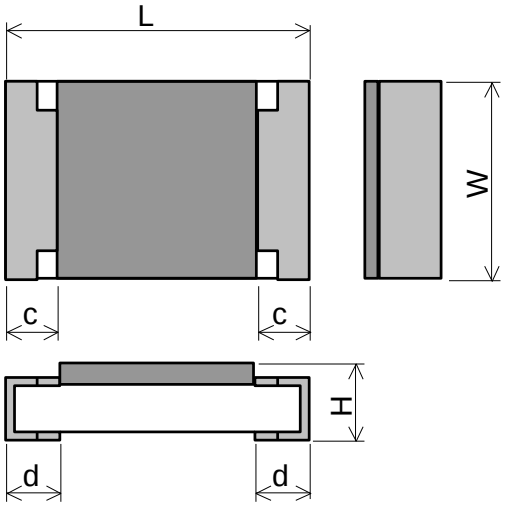
The standard packaging form shall be in accordance with Table–2.

Table–2

Symbol	Packaging form		Standard packaging quantity / units
B	Bulk (loose package)		1,000 pcs.
PA	Press pocket taping (paper taping)	8mm width, 2mm pitches	15,000 pcs.

5. Dimensions

5.1 The resistor shall be of the design and physical dimensions in accordance with Figure–2 and Table–3.



Figure–2

Table–3 Unit : mm

Style	L	W	H	c	d
RMAW06	0.6±0.03	0.3±0.03	0.23±0.03	0.1±0.05	0.15±0.05

6. Marking

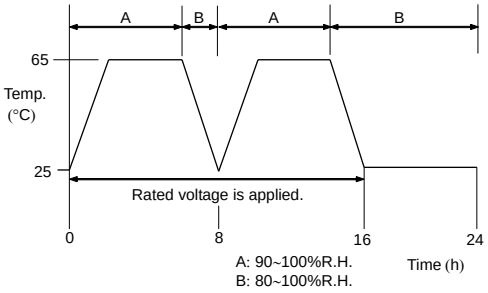
The Rated resistance of RMAW06 should not be marked.

7. Performance

7.1 The standard condition for tests shall be in accordance with Sub–clause 4.2, JIS C 5201–1: 2011

7.2 The performance shall be satisfied in Table–4.

Table–4(1)

<table>
<tr><th>No.</th><th>Test items</th><th>Condition of test (JIS C 5201–1)</th><th>Performance requirements</th></tr>
<tr><td>1</td><td>Resistance</td><td>Sub–clause 4.5</td><td>As in 4.5.2
The resistance value shall correspond with the rated resistance taking into account the specified tolerance.
Chip jumper: 50mΩ max.</td></tr>
<tr><td>2</td><td>Temperature characteristic of resistance</td><td>4.8
Natural resistance change per change in degree centigrade.
$TCR(10^{-6}/\Omega)= \frac{R2-R1}{R1(t2-t1)} \times 10^6$
t1 : 20°C $^{+5}_{-1}$ °C, t2: 155°C $^{+5}_{-1}$ °C
R1 : Resistance at t1 temperature
R2 : Resistance at t2 temperature</td><td>See Table–1.</td></tr>
<tr><td>3</td><td>Resistance to soldering heat</td><td>MIL-STD-202 Method 210
Test by a piece.
Temp. of solder bath: 270±5°C
Immersion time: 10±1s
After immersion into solder, leaving at the room temp. for 1h or more and then measure the resistance.</td><td>Resistor: ΔR/R: Within ±(0.5%+0.05Ω)
Chip jumper: 50mΩ max.
No evidence of appearance damage.</td></tr>
<tr><td>4</td><td>Solderability</td><td>J-STD-002
• Pre-condition: 155°C, 4h
Temp. of solder bath: 235°C
Immersion time: 5s
• Pre-condition: Steam aging, 1h
Temp. of solder bath: 260°C
Immersion time: 7s</td><td>The surface of terminal immersed shall be min. of 95% covered with a new coating of solder.</td></tr>
<tr><td>5</td><td>Temperature cycling</td><td>JESD22 Method JA-104
Test cycle: 1000 cycles for duty cycle as specified below.
<table>
<tr><th>Step</th><th>Temperature(°C)</th><th>Time(min)</th></tr>
<tr><td>1</td><td>–55</td><td>5~10</td></tr>
<tr><td>2</td><td>+125</td><td>5~10</td></tr>
</table></td><td>Resistor: ΔR/R: Within ±(2%+0.05Ω)
Chip jumper: 50mΩ max.
No evidence of appearance damage.</td></tr>
<tr><td>6</td><td>Moisture Resistance</td><td>MIL-STD-202 Method 106
Test condition: 10cycles for duty cycle as shown as below.
 
</td><td>Resistor: ΔR/R: Within ±(2%+0.1Ω)
Chip jumper: 50mΩ max.
No evidence of appearance damage.</td></tr>
</table>

Table−4(2)

No	Test items	Condition of test (JIS C 5201−1)	Performance requirements
7	Operational life	MIL-STD-202 Method 108 Test temp.: 125±2°C Test power: 35% of rated power shall be applied for continuously. Test period: 1,000 $^{+48}_{0}$ h	Resistor: ΔR/R: Within ±(3%+0.1Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
8	Bias humidity	MIL-STD-202 Method 103 Test condition: 85°C & 85% R.H. Test power: 10% of rated power shall be applied for continuously. Test period: 1,000 $^{+48}_{0}$ h	Resistor: ΔR/R: Within ±(3%+0.1Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
9	High Temperature exposure	MIL-STD-202 Method 108 Test condition: 155±2°C Test period: 1,000 $^{+48}_{0}$ h	Resistor: ΔR/R: Within ±(3%+0.1Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
10	Substrate bending test	AEC-Q200-005 Bent value: 2 mm(Among the fulcrums: 90mm) Duration: 10s	Resistor: ΔR/R: Within ±(1%+0.05Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
11	Adhesion	AEC-Q200-006 Force: 3N Duration: 60 s±1 s	No remarkable damage or removal of the terminations
12	Mechanical Shock	MIL-STD-202 Method 213 Peak acceleration: 1500g Peak Half sine pulse Velocity 15.4ft/sec The shock specified above shall be applied in each direction of 3 mutually perpendicular axis (3 total of 18 shocks).	The resistance value shall correspond with the rated resistance taking into account the specified tolerance. No evidence of appearance damage.
13	Vibration	MIL-STD-202 Method 204 Peak acceleration: 5g's Each direction of 3 mutually perpendicular axis. Test cycle: 12 Cycles	Resistor: ΔR/R: Within ±(1%+0.05Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
14	Thermal shock	MIL-STD-202 Method 107 Test cycle: 300 cycles for duty cycle as specified below.	Resistor: ΔR/R: Within ±(2%+0.1Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
		Step / Temperature(°C) / Time(min) 1 / −55 / 15 2 / +125 / 15 Max transfer time: 20s	
15	ESD test	AEC-Q200-200 Test condition: 300V	Resistor: ΔR/R: Within ±(1%+0.05Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
16	Hydrogen sulphide test	H2S concentration: 3ppm Test temp.: 40°C Relative humidity: 90% Test period: 1000h	Resistor: ΔR/R: Within ±(1%+0.05Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.

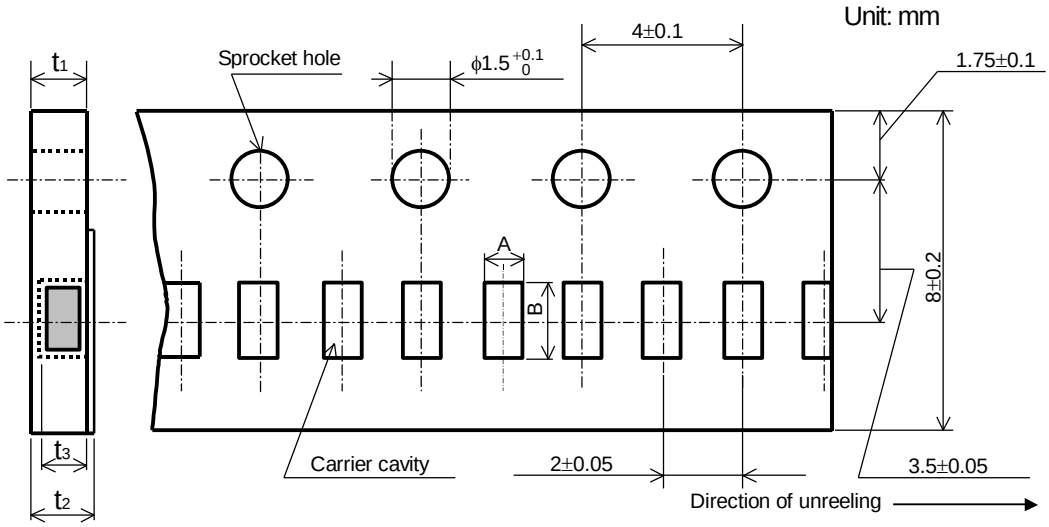
8. Taping

8.1 Applicable documents JIS C 0806–3: 2014, EIAJ ET–7200C: 2010

8.2 Taping dimensions

Press pocket taping (Paper taping, 8mm width, 2mm pitches)

Taping dimensions shall be in accordance with Figure–3 and Table–5.



Figure–3

Table–5 Unit: mm

Style	A	B	t_1	t_2	t_3
RMAW06	0.37±0.05	0.67±0.05	0.42±0.03	0.45±0.05	0.27±0.02

1). The cover tapes shall not cover the sprocket holes.

2). Tapes in adjacent layers shall not stick together in the packing.

3). Components shall not stick to the carrier tape or to the cover tape.

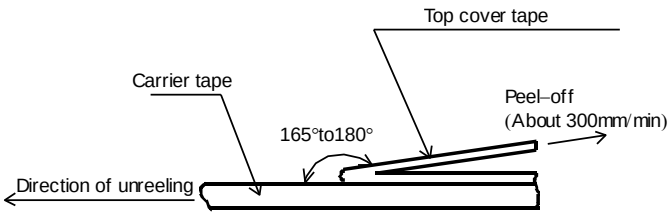
4). Pitch tolerance over any 10 pitches ±0.2mm.

5). The peel strength of the top cover tape shall be with in 0.1N to 0.5N on the test method as shown in the following RMAW06: Figure–4.

6). When the tape is bent with the minimum radius for 25 mm the tape shall not be damaged and the components shall maintain their position and orientation in the tape.

7). In no case shall there be two or more consecutive components missing.
The maximum number of missing components shall be one or 0.1%, whichever is greater.

8). The resistors shall be faced to upward at the over coating side in the carrier cavity.

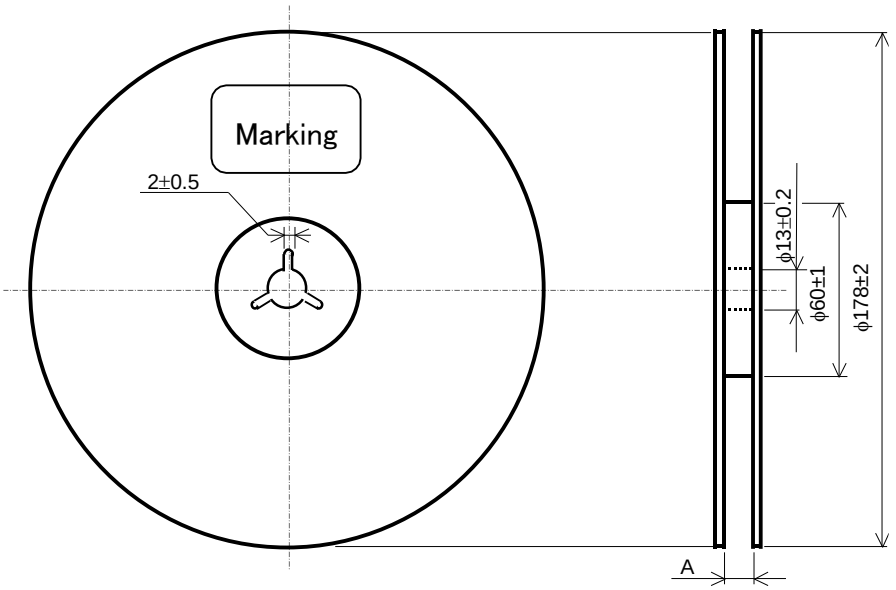


Figure–4

8.3 Reel dimension

Reel dimensions shall be in accordance with the following Figure–5 and Table–6.

Unit: mm



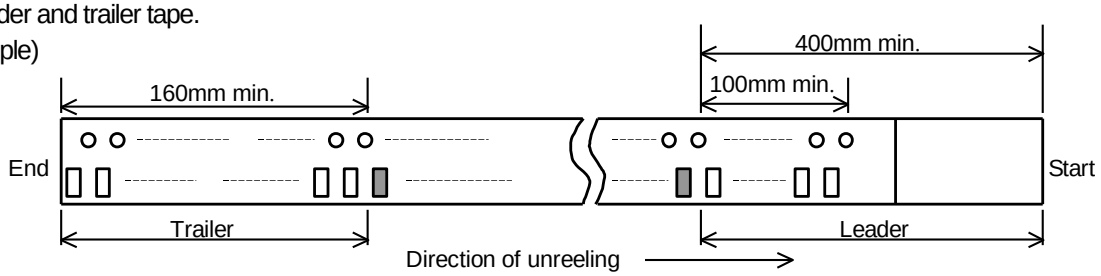
Figure–5

Table–6 Unit: mm

Style	A
RMAW06	9±0.5

8.4 Leader and trailer tape.

(Example)



Figure–6

9. Marking on package

The label of a minimum package shall be legibly marked with follows.

(1) Classification (Style, Temperature coefficient of resistance, Rated resistance, Tolerance on rated resistance, Packaging form)

(2) Quantity (3) Lot number (4) Manufacturer's name or trade mark (5) Others